REMARKS

This Amendment responds to the Office Action dated December 29, 2005 in which the Examiner rejected claims 1-6 under 35 U.S.C. §102(b) and rejected claims 7-9 under 35 U.S.C. §103.

Applicant respectfully thanks the Examiner for acknowledging the Information Disclosure Statement filed August 4, 2003. However, a corrected PTO-1449 was filed on September 9, 2003, copy attached along with stamped postcard. Applicants respectfully request the Examiner acknowledge the corrected Information Disclosure Statement which corrects the document number for the first listed foreign patent document.

As indicated above, claim 1 has been amended to depend from claim 3, claim 3 has been rewritten into independent form and incorporates part of claim 4 and claim 4 has been accordingly amended. The amendment is unrelated to a statutory requirement for patentability.

Claim 3 claims a semiconductor integrated circuit comprising a plurality of modules having their operations controlled by respective chip select signals. Each module has a plurality of memory cells and each module has a control circuit controlling an operation of reading or writing data from or into the memory cell. The plurality of modules receive a common address signal sent through a common internal address bus, where the plurality of modules have word lines different in number. The control circuit included in a module that does not have a maximum number of word lines controls an operation of reading or writing data from or to the memory cell in a test mode, irrespective of a value of the chip select signal, only

when values of one or more prescribed bits forming an address signal are prescribed values.

Through the structure in the claimed invention having a) a plurality of modules having word lines different in number and b) a control circuit, included in a module that does not have a maximum number of word lines, controls an operation of reading or writing data in a test mode irrespective of a value of a chip select signal, only when values of one or more prescribed bits forming an address signal are prescribed values, as claimed in claim 3, the claimed invention provides a semiconductor integrated circuit which prevents the same word line from being activated at different times in a memory test mode. The prior art does not show, teach or suggest the invention as claimed in claim 3.

Claims 1-3 and 6-9 were rejected under 35 U.S.C. §102(b) as being anticipated by *Urakawa et al.* (U.S. Patent 6,324,106).

Applicants respectfully traverse the Examiner's rejection of the claims under 35 U.S.C. §102(b). The claims have been reviewed in light of the Office Action, and for reasons which will be set forth below, Applicants respectfully request the Examiner withdraws the rejection to the claims and allows the claims to issue.

As discussed above, since claim 3 now claims a plurality of modules having word lines different in number and a control circuit controls an operation of reading or writing irrespective of a chip select signal only when values of one or more prescribed bits forming an address signal are prescribed values (in a module that does not have a maximum number of word lines) as claimed in original claim 4, applicants respectfully request the Examiner withdraws the rejection to claim 3 under

35 U.S.C. §102(b) and withdraws the rejection to claims 1 and 6-9 under 35 U.S.C. §102(b).

Claims 1-6 were rejected under 35 U.S.C. §102(b) as being anticipated by *Kawamata* (U.S. Publication No. 2001/0042231).

Kawamata appears to disclose [0001] the structure of a fail information memory in a memory testing apparatus and a memory testing method using a fail information memory. [0050] Referring to FIG. 5, there is shown a block diagram illustrating the arrangement of the fail information memory in an embodiment of the memory testing apparatus. For a plurality of comparator channels "0" to "3", the embodiment shown in FIG. 5 includes a plurality of fail information memories 110 to 113 for a main cell array, and one fail information memory 20 for the redundant cells. [0059] A redundancy signal is supplied to a write enable terminal WEB (where the tail end character "B" indicates a low active signal) of the fail information memory 110. When this redundancy signal is at a low level, it indicates that the memory cell testing is carried out for the main cell array of the semiconductor memory of the device under test, and the fail information memory 110 is put in a write enable condition. On the other hand, when the redundancy signal is at a high level, it indicates that the memory cell testing is carried out for the redundant cells of the semiconductor memory of the device under test, and the write enable terminal WEB of the fail information memory 110 is inactivated so that the fail information memory 110 is put in a condition unable to write. [0060] The fail information memories 111 to 113 for the other channel data bits D1 to D3 are constructed similarly to the fail information memory 110 for the channel data bit D0. [0061] The redundancy signal is also supplied to an inverter 50, an output of which is connected to a write enable

terminal WEB of the fail information memory 20. Therefore, when the redundancy signal is at the high level, the write enable terminal WEB of the fail information memory 20 is brought into the low level, so that the fail information memory 20 is put in a write enable condition. On the other hand, when the redundancy signal is at the low level, the write enable terminal WEB of the fail information memory 20 is inactivated so that the fail information memory 20 is put in a condition unable to write.

Thus, *Kawamata* merely discloses at paragraph [0059], a redundant signal supplied to a write enable terminal of a fail information memory 110. Nothing in *Kawamata* shows, teaches or suggests a) a plurality of modules have word lines different in number or b) a control circuit, included in a module that does not have a maximum number of word lines, controls an operation in a test mode for reading or writing irrespective of a value of a chip select signal, only when values of one or more prescribed bits forming an address signal are prescribed values as claimed in claim 3. Rather, *Kawamata* merely discloses a redundancy signal is supplied to a write enable terminal of a failed information memory 110.

Additionally, *Kawamata* merely discloses a redundancy signal is also supplied to an inverter 50, an output of which is connected to a write enable terminal of the fail information memory 20 so that the write enable terminal of the memory 20 is brought to a low level to put the memory in a write enable condition or is inactivated when the redundancy signal is at a low level [0061]. Nothing in *Kawamata* shows, teaches or suggests a) a plurality of modules have word lines different in number and b) a control circuit, included in a module that does not have a maximum number of word lines, controls a read/write operation in a test mode irrespective of a value of a chip

select signal, only when values of one or more prescribed bits forming an address signal are prescribed values as claimed in claim 3. Rather, *Kawamata* merely discloses in paragraph [0061] placing the fail information memory 20 in a write enable condition when a redundancy signal is high and placing the memory in an inactive condition when the redundancy signal is low.

Since nothing in *Kawamata* shows, teaches or suggests the primary features as claimed in claim 3, Applicants respectfully request the Examiner withdraws the rejection to claim 3 under 35 U.S.C. §102(b).

Claims 1, 4 and 6-9 depend from claim 3 and recite additional features. Applicants respectfully submit that claims 1, 4 and 6-9 would not have been anticipated by *Kawamata* within the meaning of 35 U.S.C. §102(b) at least for the reasons as set forth above. Therefore, Applicants respectfully request the Examiner withdraws the rejection to claims 1, 4 and 6-9 under 35 U.S.C. §102(b).

Claims 7-9 were rejected under 35 U.S.C. §103 as being unpatentable over *Kawamata* and further in view of *Urakawa*.

Applicants respectfully traverse the Examiner's rejection of the claims under 35 U.S.C. §103. The claims have been reviewed in light of the Office Action, and for reasons which will be set forth below, Applicants respectfully request the Examiner withdraws the rejection to the claims and allows the claims to issue.

As discussed above, since nothing in *Kawamata* shows, teaches or suggests the primary features as claimed in claim 3, Applicants respectfully submit that the combination of the primary reference with the secondary reference to *Urakawa* would not overcome the deficiencies of the primary reference. Therefore, Applicants

respectfully request the Examiner withdraws the rejection to claims 7-9 under 35 U.S.C. §103.

The prior art of record, which is not relied upon, is acknowledged. The references taken singularly or in combination do not anticipate or make obvious the claimed invention.

Thus, it now appears that the application is in condition for reconsideration and allowance. Reconsideration and allowance at an early date are respectfully requested.

If for any reason the Examiner feels that the application is not now in condition for allowance, the Examiner is requested to contact, by telephone, the Applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed within the currently set shortened statutory period, Applicants respectfully petition for an appropriate extension of time. The fees for such extension of time may be charged to Deposit Account No. 02-4800.

In the event that any additional fees are due with this paper, please charge our Deposit Account No. 02-4800.

Respectfully submitted,

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